IN THE CLAIMS:

Please cancel claims 6 and 7. **Please also amend** claims 1-3 and 8-11, and **add new claims** 12 and 13, as shown in the complete list of claims that is presented below.

1. (currently amended): A semiconductor device comprising:

an N type polysilicon gate and a P type polysilicon gate, both ~~disposed~~ etched simultaneously, together occupying a first total area; and

a non-doped polysilicon body disposed ~~contiguous~~ adjacent to at least one of the N type polysilicon gate and the P type polysilicon gate, the non-doped polysilicon body occupying a second area larger than the first total area of the N type and P type polysilicon gates.

2. (currently amended): The semiconductor device according to claim 1, wherein impurities for the N type polysilicon gate and the P type polysilicon gate comprise ~~phosphor~~ phosphorus and boron respectively.

3. (currently amended): A dry etching method for a semiconductor device, comprising the following steps of:

simultaneously gate-etching an N type polysilicon gate and a P type polysilicon gate; and

setting an etching area occupied by a non-doped polysilicon body, which is ~~contiguous~~ adjacent to at least one of the N type polysilicon gate and the P type polysilicon gate, larger than a total area of the N type polysilicon gate and the P type polysilicon gate.

4. (previously presented): The dry etching method according to claim 3, wherein said gate etching comprises two-stage etching.

5. (original): The dry etching method according to claim 4, wherein the two-stage etching includes a first stage using a mixed gas of HBr and O_2 and a second stage using a mixed gas of HBr, O_2 and He.

Claims 6 and 7 (cancelled).

8. (currently amended): The semiconductor device according to claim 1, ~~comprising a plurality of~~ wherein the N type polysilicon gate and the P type polysilicon gate are disposed ~~in mixed form~~ adjacent one another.

9. (currently amended): The dry etching method according to claim 3, wherein the step of simultaneously gate-etching the N type polysilicon gate and the P type polysilicon gate further comprises also etching the non-doped polysilicon body along with ~~gate etching to form gate electrodes on~~ the N type polysilicon gate and the P type polysilicon.

10. (currently amended): The dry etching method according to claim 9, wherein the ~~gate electrodes are smaller in area than the~~ N type polysilicon gate or the P type polysilicon gate are adjacent one another.

11. (currently amended): The dry etching method according to claim 3, ~~comprising forming a plurality of~~ wherein the N type polysilicon gate and the P type polysilicon gate are disposed ~~in mixed form~~ adjacent one another.

12. (new): The semiconductor device of claim 1, wherein the N type polysilicon gate, the P type polysilicon gate, and the non-doped polysilicon body are all etched simultaneously from a single polysilicon layer.

13. (new): The dry etching method of claim 3, wherein the N type polysilicon gate, the P type polysilicon gate, and the non-doped polysilicon body are all etched simultaneously from a single polysilicon layer.